1 / 18

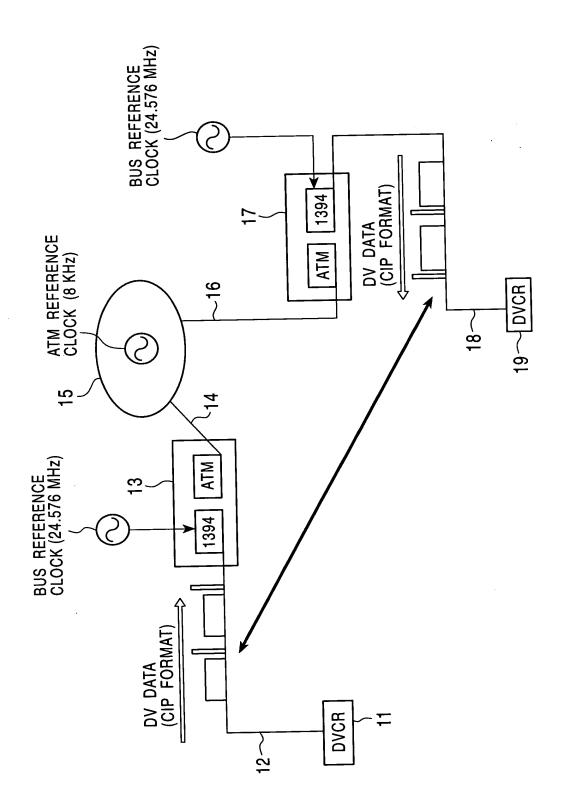
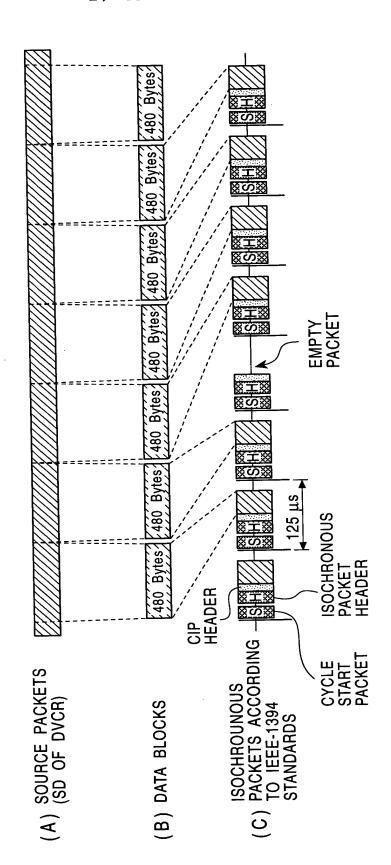


FIG. 2



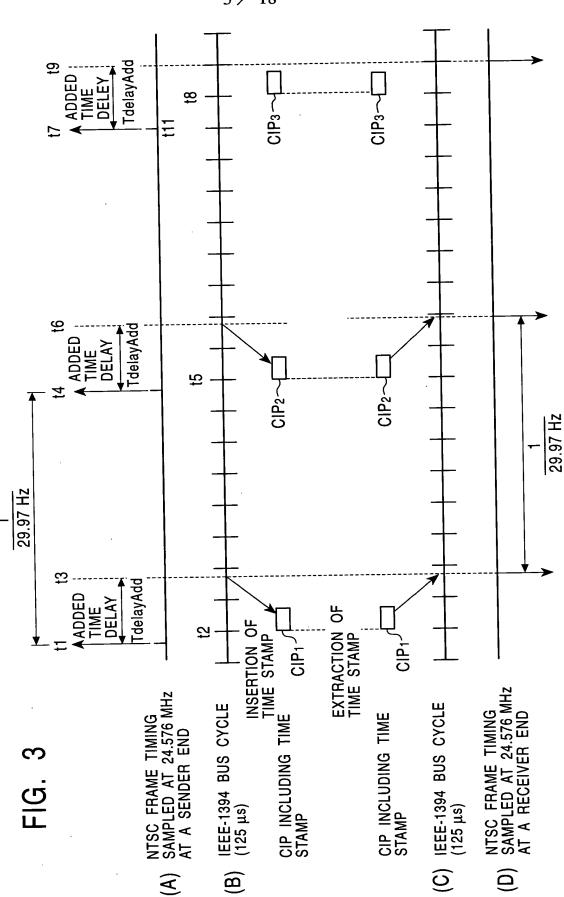
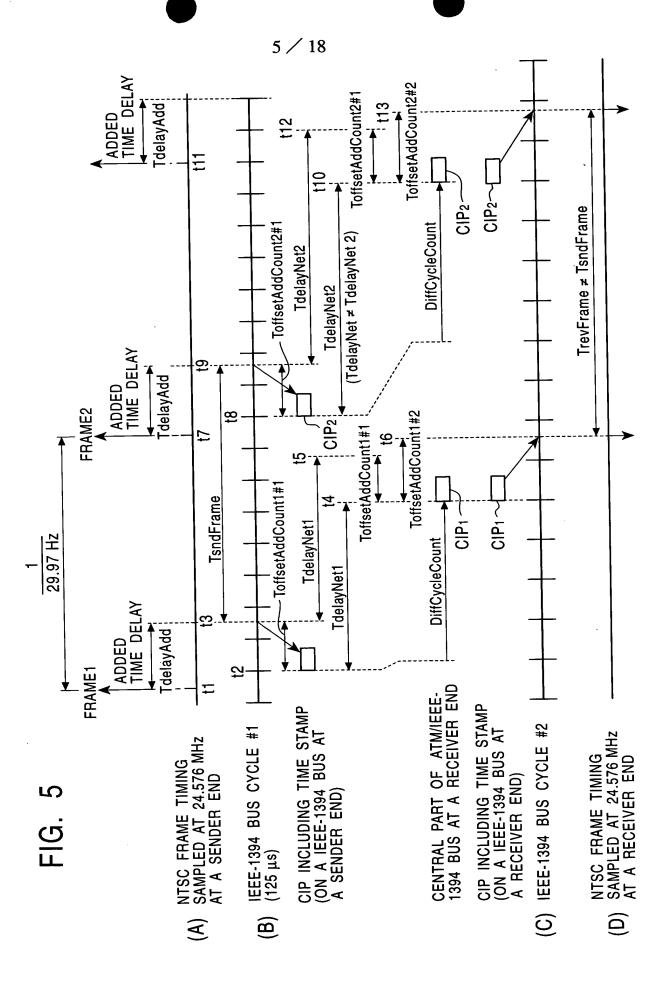
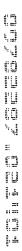


FIG. 4

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GENERATES | IEEE-1394 BUS REFERENCE CYCLE START PACKETS TRANSMITTED SYNCHRONOUSLY 42A SDH FRAME PULSE (8 KHz) 24.576 MHz DV DATA (CIP FORMAT) 1394 42 ATM 9 DVCR 15A 18 SDH FRAME PULSE (8 KHz) GENERATES IEEE-1394 BUS REFERENCE CLOCK IN SYNCHRONIZATION WITH AN ATM NETWORK 5 ATM 1394 24.576 MHz (∕ CYCLE START PACKETS TRANSMITTED SYNCHRONOUSLY (1/3072=8 KHz) DV DATA (CIP FORMAT) DVCR 12

FG.

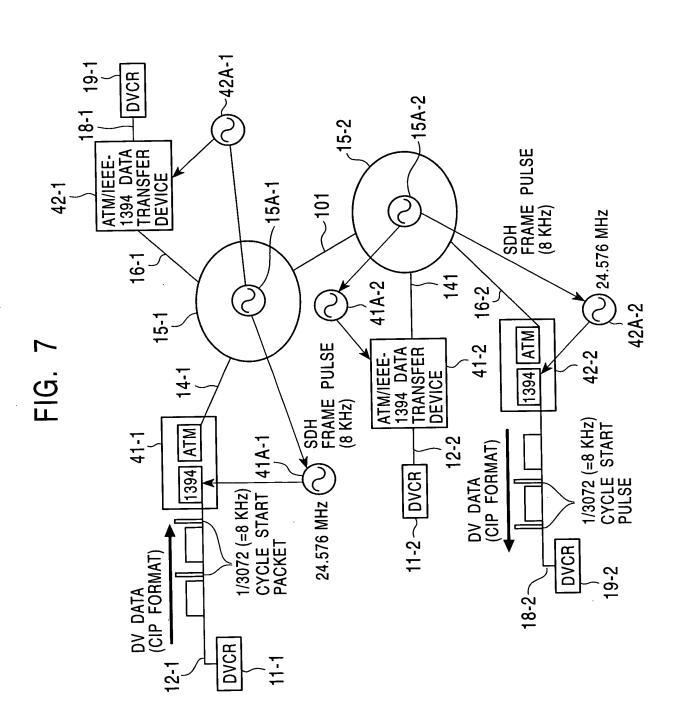
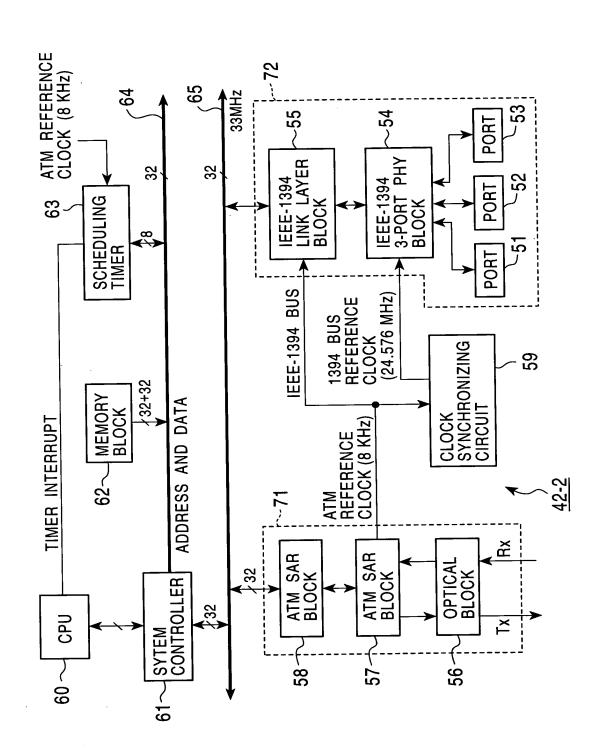
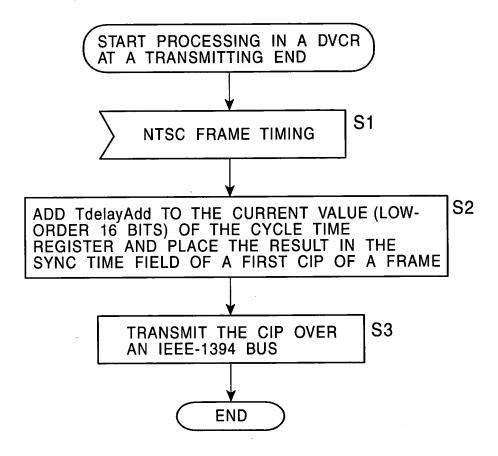


FIG. 8



VCXO (24.576 MHz) 84 FILTER 23 83 PHASE COMPARA-TOR 82 8 KHz FREQUENCY DIVIDER (1/3072) ₩. ATM REFERENCE_CLOCK (8 KHz)

FIG. 10

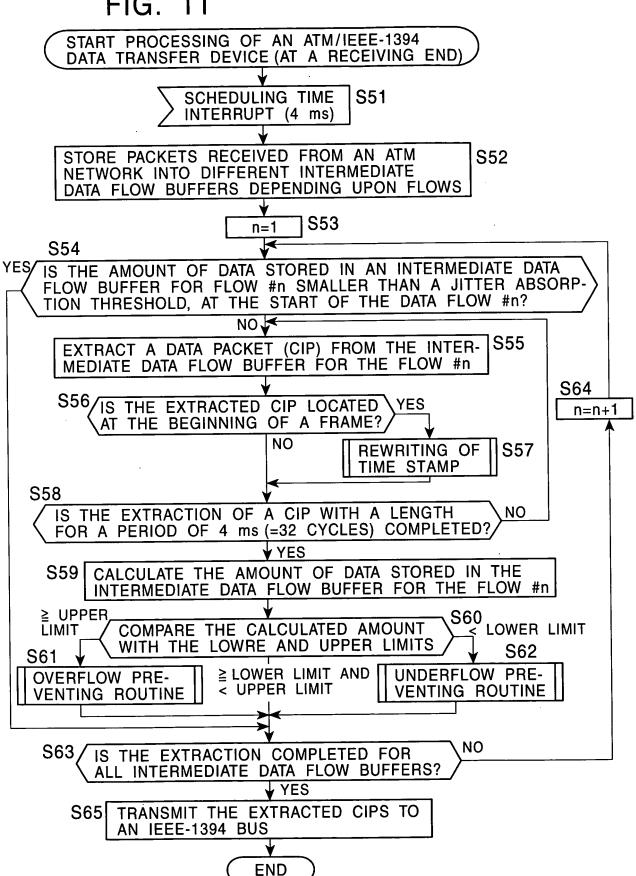


į, <u>.</u>

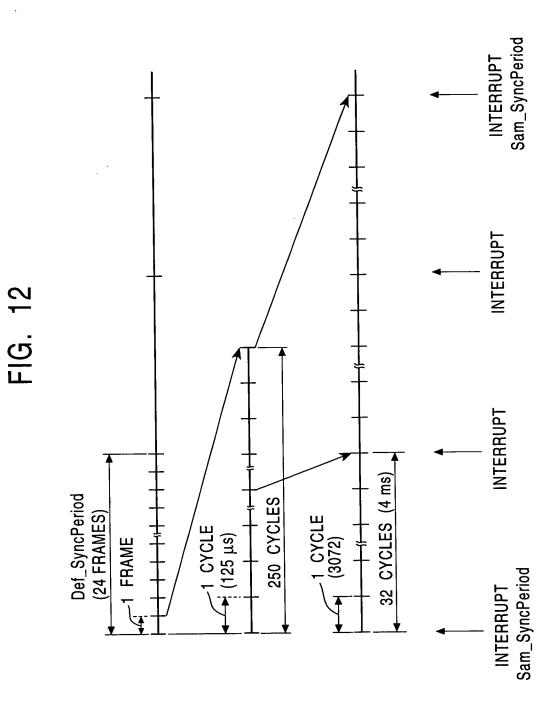
– ÕDLON, SPIVAK, F,T AL DOCKET #: 203253US6 INV: Takashi NOMURA SHEET <u>11</u> OF <u>18</u>

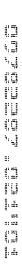
11 / 18

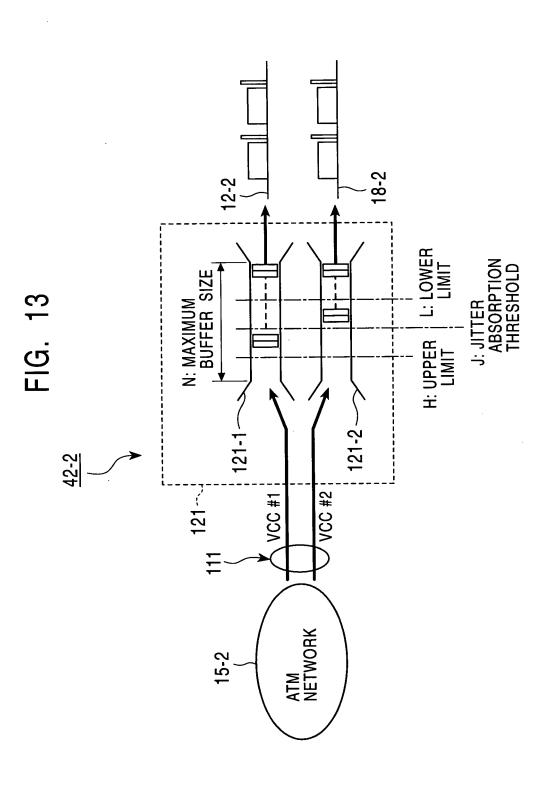
FIG. 11





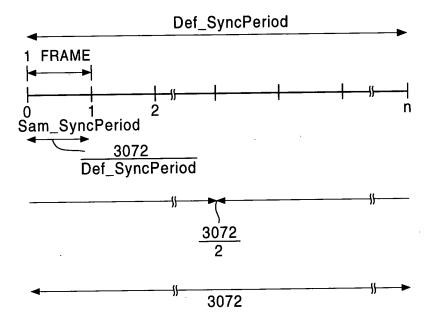






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FIG. 15



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FIG. 16

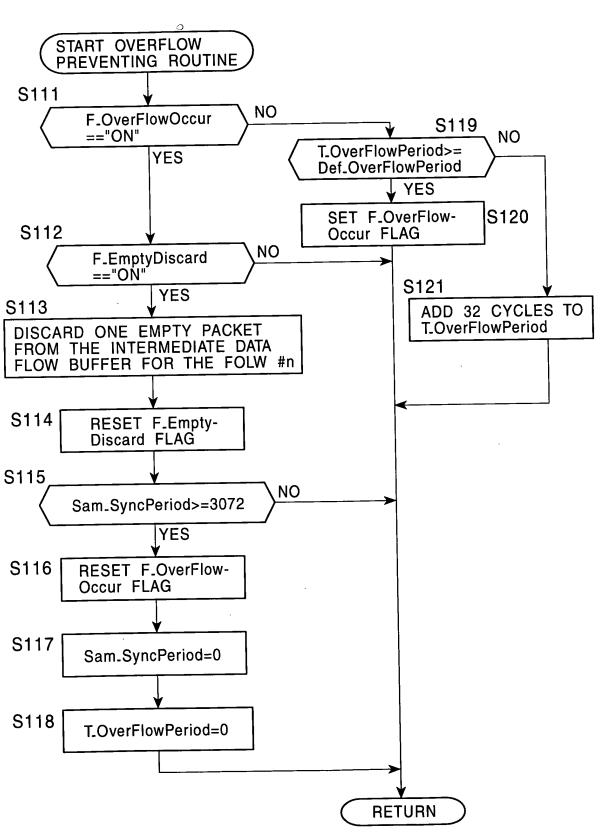


FIG. 17

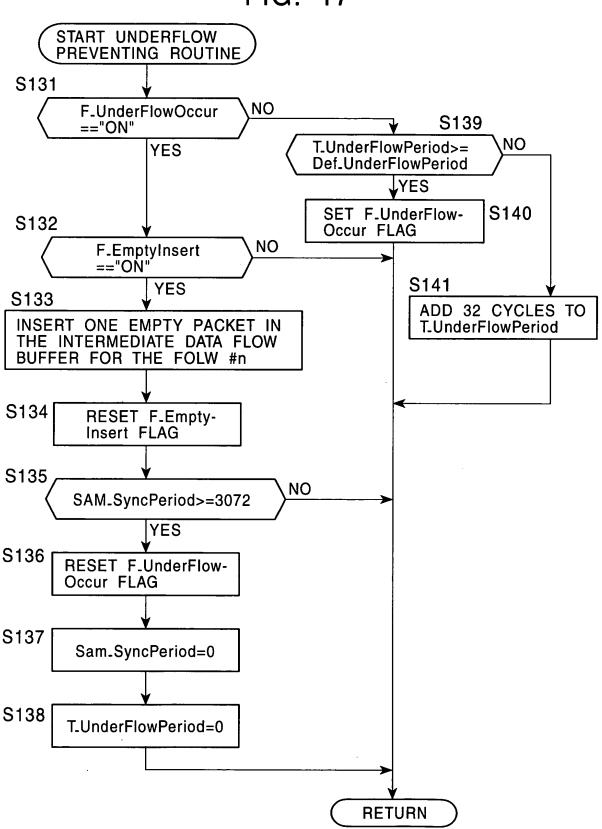


FIG. 18

